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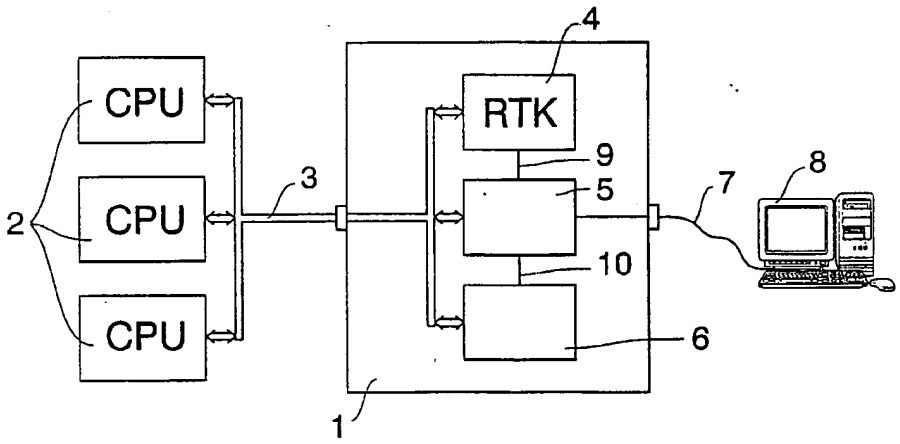
(54) Title: AN INTEGRATED CIRCUIT



(57) Abstract: An integrated circuit (1) for a computer system, where the computer system comprises at least one processor (2) and an operating system which has at least one part (4) implemented in hardware, wherein said operating system part (4) is arranged in the integrated circuit (1). The integrated circuit (1) further comprises a unit (5) for supervising events in said computer system, wherein the supervising unit (5) has means for detecting events in the computer system and means for recording information about the events and that the supervising unit (5) is connected to said operating system part (4) in such a manner that information about internal events in the operation system part is possible to transfer to the supervising unit.

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AN INTEGRATED CIRCUIT

DESCRIPTION

FIELD OF THE INVENTION

The present invention refers to an integrated circuit for a computer system comprising at least one processor and an operating system, which at least has a part that is implemented in hardware, wherein said operating system part is arranged on the integrated circuit.

PRIOR ART

In a computer system, it is desirable to be able to detect and record different events in the computer system for the purpose of analyzing, measuring the performance, and testing the computer system. This is particularly important during the development of a new system. From now on, supervising of a computer system relates to the collection of information regarding the behavior of the computer system. The supervision may also extract or validate design parameters, such as execution times and delays in the system.

It is known to supervise what happens in a computer system through specific program instructions being located in the software code of the system. When those instructions are executed, events are initiated, and information about the generated events is stored for later analysis. A drawback with handling the supervision by software instructions in the program code is that the software of the system becomes overloaded with those extra instructions and that they might influence the timing in the system.

The introduced disturbances caused by the extra instructions might also change the behavior of the program and when the software test is completed and the extra instructions are removed new errors might occur due to the change of the timing.

It is particularly important in a real-time operating system that the supervision does not influence the timing. Real-time systems are different from most other systems, since they are tremendously sensitive to disturbances in the timing. Typical for a real-time operating system is that it is deterministic, which means that it shall always be predictable. Thus, the supervision of a real-time system is not allowed to change the timing or the order of events in the system.

Another known method for supervising a computer system is the use of a supervisory device implemented in hardware. Such a supervisory device comprises probes, which are connected to buses and signals in the computer system. The supervisory device detects passively what is going on at the bus and collects information about events, which might be of interest. The advantage with hardware supervision is that it does not interfere with the system that it supervises. A problem in connection with the use of a separate supervisory device is that, in certain modern computer systems, many functions are physically integrated in the same circuit in the same enclosure. Therefore, it may be impossible to reach all signals necessary to achieve a good supervision. The enclosure of an integrated circuit should preferably not be too large and thus it has a limited number of pins. To obtain all signals necessary for the supervision, the number of pins must be considerably increased and thus the size of the enclosure must be increased and that is not desirable.

For the purpose of enhancing the performance in a computer system, it is known to implement the whole or at least a part of the operating system in hardware in an external unit outside the processor. High performance is particularly important in applica-

tions performed in real-time, such as, for example in process control applications. A hardware operating system has a real-time kernel arranged on an integrated circuit that is physically separated from the processor and the real-time kernel is communicating with the processor via a bus connection. It is not suitable to supervise such a computer system with software, since the timing in the system might be influenced. It is true that a supervisory device can be connected to the bus between the processor and the hardware operating system, but the information accessible on the bus is not enough to perform a reliable supervision of the system or to detect errors in the program code.

SUMMARY OF THE INVENTION

The object of the inventions is to provide an integrated circuit comprising a hardware operating system or at least a part of an operating system which is implemented in hardware and which makes it possible to achieve a reliable supervision of events in the computer system.

This object is achieved with the initially described integrated circuit, which is characterized in that it further comprises a unit for supervising events in said computer system, wherein the supervising unit has means for detecting events in the computer system and means for recording information about the events, and that the supervising unit is connected to said operating system part in such a manner that information about internal events in the operating system part is possible to transfer to the supervising unit. By arranging a supervising unit in the same integrated circuit as a hardware operating system part and connecting them to each other, necessary information for the supervision, for example information about internal events in the operating system part, can be transferred to the supervising unit. Such internal information is not obtainable on the bus between the processor and the operating system part. The information

about internal events is usually inaccessible or so sensitive to disturbances, such as capacitances in the cables, that it is not measurable. The supervising unit is passive and listens to what is going on in the operating system without influencing the system and its timing. When the supervising unit has detected an interesting event, it records the information about the event. This information may later be analyzed, for instance for the purpose of detecting errors. Since the supervising unit is implemented in hardware, nothing prevents it from being used for supervision of arbitrary physical signals in the system.

In a preferred embodiment of the invention, said operating system is a real-time operating system and said operating system part is a real-time kernel. The invention is particularly advantageous if the operating system is a real-time operating system, since the timing in the system is not influenced by the supervision according to the invention.

In an embodiment of the invention, the operating system part comprises means for handling when a number of tasks shall be executed by the processor and said information comprises information about the current state of the tasks. This is important information and knowledge about it contributes to an improved supervision of the system. This information is difficult to obtain outside the integrated circuit, but the fact that the supervising unit and the hardware operating system part are arranged on the same integrated circuit makes it possible to transfer this information to the supervising unit in a simple way.

In an embodiment of the invention, the operating system part is communicating with one or a plurality of processors via a bus and the supervising unit comprises means for receiving information from the processor/processors from said bus. Thanks to the fact that the supervising unit is connected to the bus, a processor can address the supervising unit and transfer information about what is going on in the processor to the supervising unit.

The software is provided with program instructions for transferring information via the bus to the supervising unit. Thus, the supervision of the software can be based on events in the operating system part and on arbitrary information generated by the software itself. Accordingly, a combination of hardware and software supervision is obtained. This means that the supervision is further improved, since the information about internal events in the operating system is supplemented with information about events in the software. Since most of the supervision is done in the hardware, only a few extra instructions in the software code are necessary and thus the load on the system is not so large as when all supervision is done in the software. Since the load on the system becomes low, the extra instructions do not necessarily have to be taken away when the supervision is finished and problems with the timing is thus avoided.

All information about events in the processor is not available on the bus. In an embodiment of the invention, the integrated circuit comprises at least one processor, which is connected to the supervising unit in such a manner that information about internal events in the processor is possible to transfer to the supervising unit. By integrating one or a plurality of processors in the computer system in the same circuit as the operative system part and the supervising unit, it is possible to transfer information about internal events in the processor to the supervising unit. Thus, further improvement of the supervision is achieved.

In an embodiment of the invention, the integrated circuit comprises means for transferring the stored information to an external unit for further analysis of the information. The external unit may, for example, be a computer. The recorded and stored events are sent through a communication link to the external unit where they are stored in a database. The collected information may later, for example, be used for event based debugging, analysis of the behavior, and for statistics.

DESCRIPTION OF THE DRAWINGS

The present invention will now be explained by the description of different embodiment and with reference to the appended drawings.

Fig. 1 shows a block diagram of a computer system with an integrated circuit according to an embodiment of the invention.

Fig. 2 shows a block diagram of a supervising unit arranged on the integrated circuit in Figure 1.

Fig. 3 shows the format of an event package.

Fig. 4 shows another embodiment of an integrated circuit according to the invention.

DESCRIPTION OF EMBODIMENTS

A computer program is structured in different tasks. A task is a sequentially arranged program and performs a predetermined function. In a real-time operating system, the tasks are given mutually priority and if two tasks are to be executed at the same time by the processor, the task with the highest priority is executed first. The means handling when a certain task is to be executed by the processor is denoted a scheduler and forms the kernel in a real-time operating system.

Figure 1 shows a computer system comprising an integrated circuit 1 according to the invention and three processors 2 arranged in parallel. The processors 2 and the integrated 1 circuit are connected to each other via a system bus. The computer system has a real-time operating system comprising a real-time kernel 4, which is implemented in hardware (RTK = Real Time Kernel) in the integrated circuit 1. The real-time kernel 4 is ar-

ranged in such a manner that it mainly executes the same functions as traditional real-time operating systems which are implemented in software do, for example handling, scheduling, and giving priority to tasks, communication, and synchronization between the tasks as well as interruption handling. More about how a real-time operating system is constructed is described in the book "Utilization of Hardware Parallelism in Realizing Real-Time Kernels" by Lennart Lind, ISBN 0280-4506.

The integrated circuit further comprises a supervising unit 5 connected to the real-time kernel 4. The function of the supervising unit is to detect and record events in the computer system. Events in the operating system is, for example:
- a system call to the operating system, such as create task, delete task, send message, receive message,
- the state of the task is changed, such as setting a task in a blocked state or unlock it from the blocking, and
- interruption request from external units.

For the purpose of supervising events in the operation system, the supervising unit 5 is connected directly in the hardware to a number of selected signals in the real-time kernel 4. The connection is implemented as one or a plurality of physical wires 9 from internal signals in the real-time kernel 4 to the supervising unit 5. In such a way, it is possible to get access to valuable information about what is happening in the operating system. Those internal signals comprise i.a. information about the condition of the tasks in the system, the priority of the tasks, internal communication activities as well as internal and external interruptions.

In certain cases, the ability to generate events from the software is necessary, for example to see whether certain control points are passed or to report the contents in a certain memory. Such events can be produced by introduction of software instructions in the program code. The supervising unit can also be used for recording general information, directly generated from the soft-

ware, i.e. information coming directly from the execution of the software on one or a plurality of processors 2 in the system. For the purpose of supervising events in the software and to receive information from the software, a supervising unit 5 is connected to the system bus 3. The software generates information through the system bus by writing data to a particular register in the supervising unit 5.

It is also possible to connect the supervising unit to an arbitrary signal or hardware unit in the integrated circuit for supervising the signal or the hardware unit. Such hardware units are buses and internal memories. This means that the supervising unit may also function as a general logic analyzer. Thus, the supervising unit 5 can be used to detect functional errors in the hardware. This is particularly useful in situations where conventional error localization methods are difficult to use, for example due to high system speeds or the fact that the signals are difficult to reach because of a limited number of pins in the integrated circuit. A hardware unit 6 in the integrated circuit 1 is connected through physical wires 10 to the supervising unit 5.

The supervising unit 5 is further connected through a parallel communication link 7 to an external computer 8. The supervising unit 5 listens passively to events, logical and/or on system level, in the real-time kernel 4 and interesting events are recorded. The recorded events are then transferred to a database in the external computer where further handling and analysis of the information occur.

The integrated circuit can either be implemented in ASIC (Application Specific Integrated Circuit) or in a programmable hardware such as FPGA (Field Programmable Gate Array). All the components are integrated on the same plate, which preferably is made of silicon.

Figure 2 shows a block scheme of the internal construction of the supervising unit 1. The supervising unit comprises an event detector 11, a timer 12, an event recorder 13, an event buffer 14, and an interface 15 to the external computer. Input signals to the supervising unit are hardwired signals 9 from the real-time kernel, signals on the system bus 3 and signals 10 from the hardware unit 6. The input signals are received by the event detector 11 that detects whether any event to be recorded has occurred. The event detector 11 is a comparator that compares the input signals with internal predetermined conditions. There are a number of conditions defining which events to be supervised and those conditions are hard coded in the event detector. The event detector detects whether an event has occurred by comparing the input signals with the predetermined conditions.

The event detector 11 comprises three different detectors 16-18 with different predetermined conditions. The first detector 16 receives the internal signals 9 from the real-time kernel and detects events in the operating system. The second detector 17 comprises a register receiving information from the software via the bus 3 and detects when information is written to the register. The third detector 18 receives the signals 10 from the other hardware units and detects events in the hardware units.

When any of the conditions is met, i.e. an event is detected; the event is reported further to the event recorder 13. The object of the event recorder is to produce a package with information about the event, which package later can be transferred through the interface 15 to the external computer. The event recorder 11 is activated by one or a plurality of start signals from the event detector and receives at the same time an identification number from the event detector. The identification number presents information to the event recorder about which signals to be packed together with the detected event. When the event recorder is activated, it creates an information package comprising the identification number of the event, the signals connected to

the event, and the time when the event was detected. The event package must have a certain predetermined format. The time is read from the timer 12 that is connected to the event recorder 13.

The event package is then stored in the internal event buffer 14. This buffer is organized as a FIFO queue, i.e. the oldest package comes out first from the queue and the newest package comes out last (FIFO = First In First OUT). At the same time as the event packages are stored in the event buffer, an indicator of a detected event is stored in a status register (not shown). The interface 15 transfers the packages to the external computer. Through the interface, the external computer may have an indication of the fact that an event has occurred and reads the event package from the event buffer 14. Indication about whether an event has been detected or not can either be obtained by reading the information in the status register or by programming the interface, so that it automatically generates a signal when new events are available in the event buffer. The size of the event buffer can be varied and depends on the application.

Sometimes one does not wish to transfer all detected events to the external computer, for example, if the number of events is large. In the event detector 11, there is a filter 19 implemented as a programmable register. The filter 19 makes it possible to choose interesting events and only letting those through. The filter 19 is connected to the interface 15 and it is possible to send instructions from the external computer to the filter about which events to be let through the filter.

Figure 3 shows an example of the design of a package having information about an event. The event package comprises three different fields of information, a first field 20 comprising the identification number of the event, i.e. information about the type of event, a second field 21 comprising the time, and a third

field 22 comprising more information about the event in the form of a plurality of parameters. An example of an event is when the processor begins and ends execution of a new task. Parameters in the third field should then comprise information about the identification number of the new task to be executed and which one of the processors to be executing the task. For the event "send message", the parameters should comprise identification number for the receiving task and a pointer to the message.

Figure 4 shows an embodiment of the invention, wherein an integrated circuit 29 comprising a processor 30, a real-time kernel 4 of the operating system, a supervising unit 5, and various other types of hardware 6. The computer system in this embodiment has only one processor and it is integrated in the same circuit as the real-time kernel 4 and the supervising unit 5. For a computer system comprising a plurality of processors, it is possible to integrate all the processors in the same circuit. The supervision unit 5 is hardwired to a number of internal signals in the processor 30. Thus, the supervising unit will have access to internal information about the events not visible on the system bus. Examples of such signals are signals to and from Cash memories in the processor. In the same way as in the previous embodiment, the supervising unit 5 is connected to internal signals in the real-time kernel 4 and to other hardware functions 6 in the circuit.

The invention is not limited to the disclosed embodiments but may be varied and modified within the scope of the following claims.

CLAIMS

1. An integrated circuit (1) for a computer system, where the computer system comprises at least one processor (2, 30) and an operating system which has at least one part (4) implemented in hardware, wherein said operating system part (4) is arranged in the integrated circuit (1), characterized in that the integrated circuit (1) further comprises a unit (5) for supervising events in said computer system, wherein the supervising unit (5) has means (11) for detecting events in the computer system and means (13) for recording information about the events and that the supervising unit (5) is connected to said operating system part (4) in such a manner that information about internal events in the operation system part is possible to transfer to the supervising unit.

2. An integrated circuit according to claim 1, characterized in that said operating system (4) is a real-time operating system and that said operating system part is a real-time kernel.

3. An integrated circuit according to claim 1 or 2, characterized in that the operating system part (4) comprises means for handling when a number of tasks shall be executed by the processor and that said information comprises information about the current state of the tasks.

4. An integrated circuit according to any of the claims 1-3, characterized in that said operating system part (4) is communicating with at least one processor (2, 30) through a bus (3) and that the supervising unit (5) comprises means (17) for receiving information about the events in the processor from the bus.

5. An integrated circuit according to any of the previous claims, characterized in that it comprises at least one processor (30), which is connected to the supervising unit (5) in such a

manner that information about internal events in the processor is possible to transfer to the supervising unit.

6. An integrated circuit according to any of the previous claims, characterized in that it comprises means (15) for transferring the recorded information to an external unit (8) for further analysis of the information.

7. An integrated circuit according to any of the previous claims, characterized in that it is composed of a system integrated on silicon.

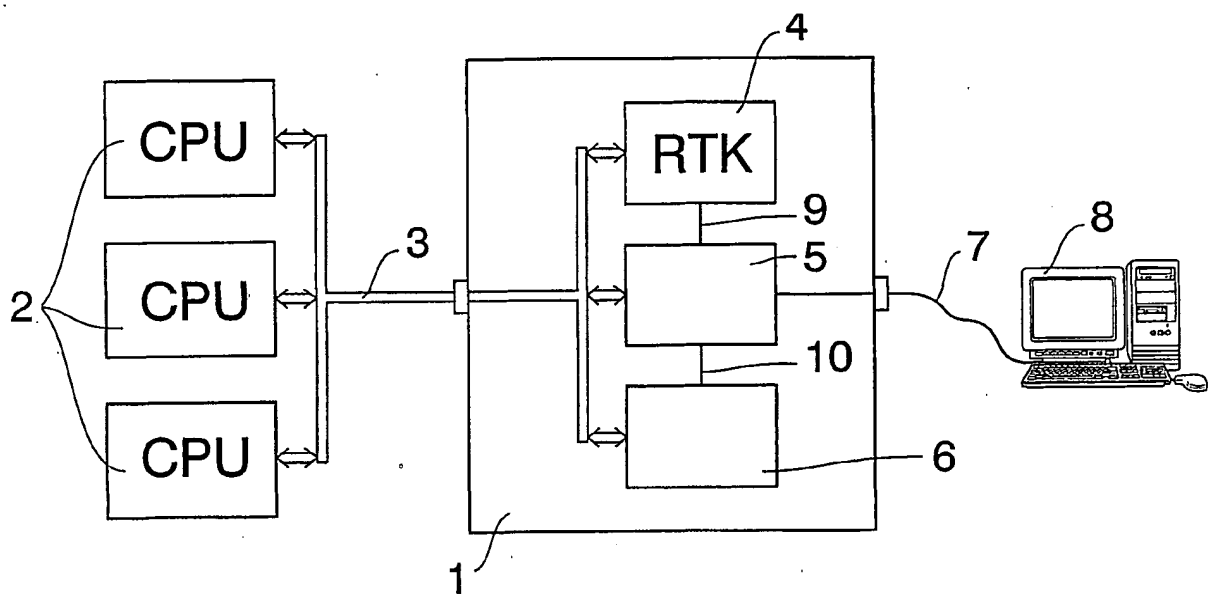

Fig. 1

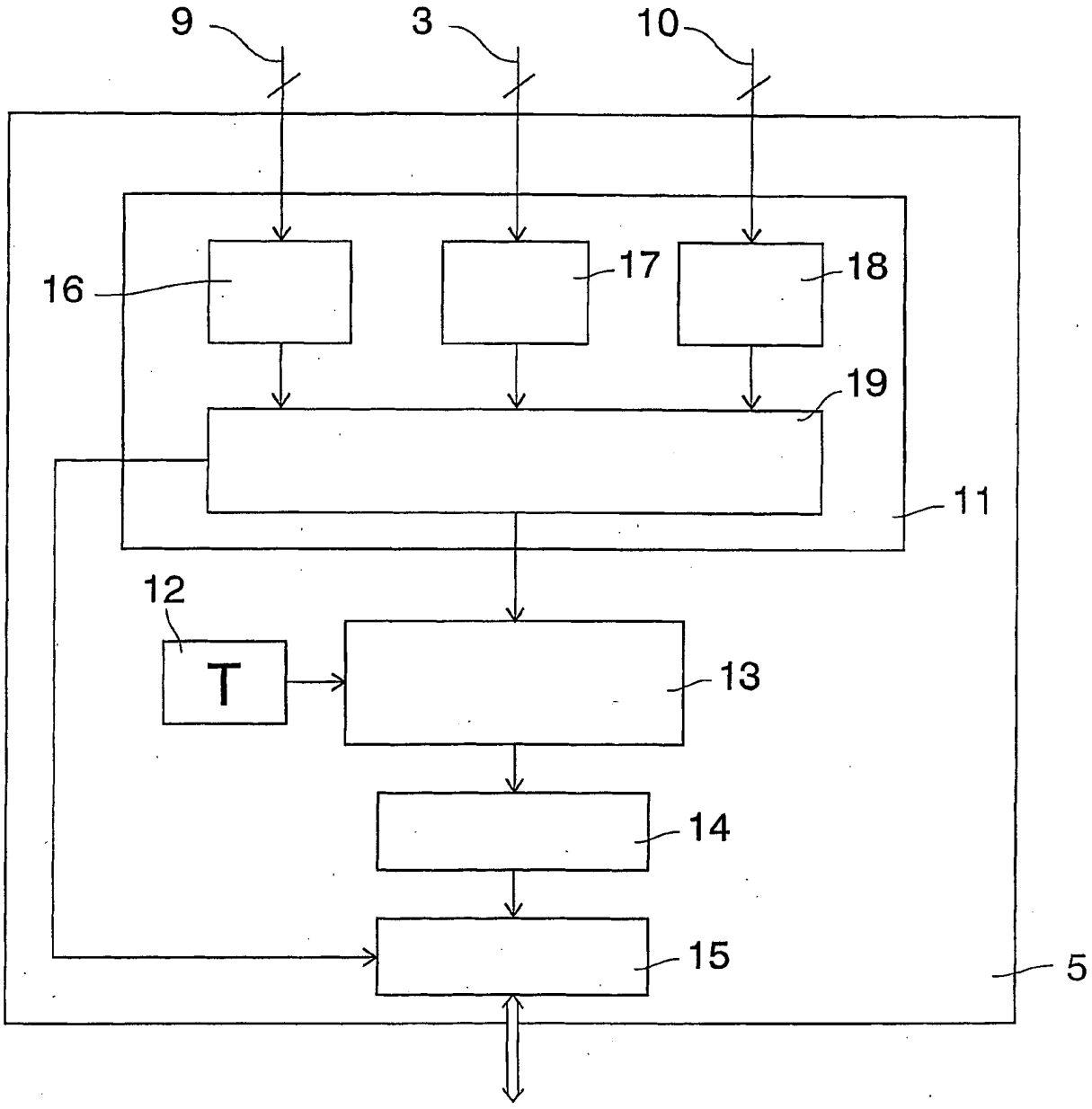

Fig. 2

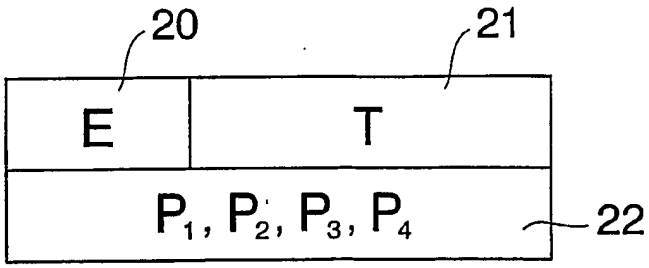

Fig. 3

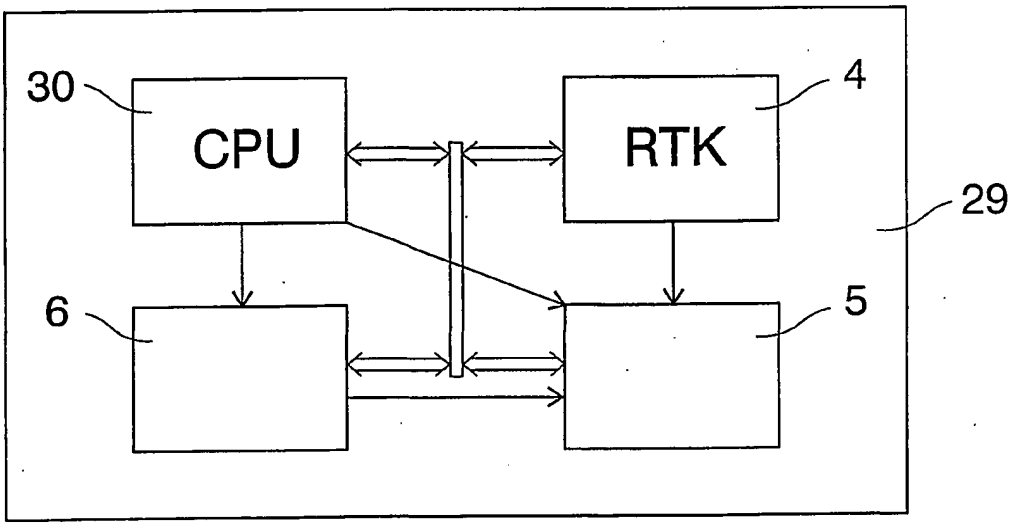

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/00561

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G06F 9/46, G06F 11/30
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, TDB, INSPEC, INTERNET

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0645705 A1 (PHILIPS ELECTRONICS UK LIMITED), 29 March 1995 (29.03.95), abstract ---	1-7
A	EP 0518573 A2 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 16 December 1992 (16.12.92), abstract ---	1-7
A	US 5355501 A (GROSS, R.A. ET AL), 11 October 1994 (11.10.94), abstract ---	1-7

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 June 2002	02-07-2002
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Pär Heimdal /OGU Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 02/00561

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
L	LINDH, Lennart et al. "Harware Accelerator for Single and Multiprocessor Real-Time Operating Systems" [on line]. Mälardalens Högskola, Sweden, June 1999 [retrieved on 2002-06-24]. Retrieved from the Internet: <URL:http://www.ce.chalmers.se/~dsa98/camera/C5_2.Pdf> --	1-7
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Concerning Box C., "DOCUMENTS CONSIDERED TO BE RELEVANT"

Cited L-Category Documents:
LINDH, Lennart et al. "Harware Accelerator for Single and Multiprocessor Real-Time Operating Systems"

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The date when the documents were made public and/or the content of the documents at the time of publication has not been further investigated or confirmed by the ISA. Thus the cited documents could not, at the present moment, be considered as part of the general state of the art. According to PCT International Search Guidelines, Chapter VI-6, the documents are referred to as L-category documents. However, the applicant is informed that further investigation on this subject might be performed by e.g. a National Patent Office and that such an investigation possibly could result in a confirmation of the content of the documents on the respective time of publication.

Cited L-Category Document:
"Publications" (selected publications), MRTC (Mälardalen Real-Time Research Center)

The cited document reveals an indication of public availability of another cited document and/ or an indication of a date when the said other cited document was made available to a large or unspecified group of people. According to PCT International Search Guidelines, Chapter VI-6, the document is referred to as an L-category document.

INTERNATIONAL SEARCH REPORT

Information on patent family members

10/06/02

International application No.
PCT/SE 02/00561

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